CLAIMS

What is claimed is:

1 1. A processor comprising:

2 a first voltage supply input port to receive a first voltage at a first voltage

3 level;

4 a second voltage supply input port to receive a second voltage;

5 a core to be powered by the first voltage; and

6 a memory region to be powered by the second voltage, the memory

7 region to store at least a portion of a state of the processor while the

8 first voltage supply is at a second voltage level.

1 2. The processor of claim 1, wherein the second voltage level is lower than the

2 first voltage level.

1 3. The processor of claim 1, wherein the second voltage level is approximately 0

2 volts.

1 4. The processor of claim 1, further comprising an L2 cache to be powered by

2 the first voltage.

1 5. The processor of claim 1, further comprising a first cache to be powered by

2 the first voltage, and a second cache to be powered by the second voltage.

P9739_AP.DOC

1 6.   The processor of claim 5, further comprising a snoop controller to be powered

2   by the second voltage, the snoop controller to snoop the second cache while

3   the first voltage supply is at the second voltage level.

1 7.   The processor of claim 5, wherein the second voltage level is a voltage level

2   that causes a processor state to be lost.

1 8.   The processor of claim 1, wherein the memory region is a portion of a cache

2   of the processor.

1 9.   A computer system comprising:

2   a fist voltage regulator to supply a first voltage at a first voltage level

3   during a first period of time and at a second voltage level during a

4   second period of time;

5   a second voltage regulator to supply a second voltage; and

6   a processor including a core to be powered by the first voltage and a

7   memory region to be powered by the second voltage, the memory

8   region to store at least a portion of a state of the processor during the

9   second period of time.

1 10. The computer system of claim 9, wherein the second voltage level is less

2   than half the first voltage level.

P9739_AP.DOC

1   11.   The computer system of claim 9, further comprising a clock to provide a clock

2   signal to the processor, the clock signal to be on during the first period of time

3   and off during the second period of time.

1   12.   The computer system of claim 9, wherein the second period of time is

2   associated with a low power state.

1   13.   The computer system of claim 12, further comprising a cache to be powered

2   by the second voltage, the cache to maintain its contents during the lower

3   power state.

1   14.   The computer system of claim 13, further comprising a snoop controller to be

2   powered by the second voltage, the snoop controller to snoop the cache

3   during the second period of time.

1   15.   The computer system of claim 12, further comprising an L1 cache to be

2   powered by the first voltage, the L1 cache to be flushed upon entering the

3   lower power state.

1   16.   The computer system of claim 9, wherein the portion of the state of the

2   processor includes a strapping options register.

P9739_AP.DOC

1   17.   The computer system of claim 9, wherein the memory region is protected by

2   error checking and correction (ECC) code.

1   18.   A method comprising:

2   triggering a processor of a computer system to enter a low power state in

3   which a first voltage supplied to a core of the processor is reduced to a

4   level that causes a state of the processor to be lost; and

5   saving at least a portion of the state of the processor to a memory region

6   of the processor upon entering the low power state, the memory region

7   to be powered by a second voltage during the low power state.

1   19.   The method of claim 18, further comprising flushing an L1 cache of the

2   processor upon entering the low power state, the L1 cache to be powered by

3   the first voltage.

1   20.   The method of claim 18, further comprising maintaining contents of a cache

2   of the processor upon entering the low power state, the cache to be powered

3   by the second voltage.

1   21.   The method of claim 20, further comprising performing a snoop of the cache

2   during the low power state.

           P9739_AP.DOC

1   22.   The method of claim 18, further comprising turning off a clock signal provided

2   to the core upon entering the low power state.

1   23.   A machine-readable medium including machine-readable instructions that, if

2   executed by a machine, cause the machine to perform the method of claim

3   18.

1   24.   A machine-readable medium including machine-readable instructions that, if

2   executed by a machine, cause the machine to perform the method of claim

3   19.

1   25.   A machine-readable medium including machine-readable instructions that, if

2   executed by a machine, cause the machine to perform the method of claim

3   21.

        P9739_AP.DOC